REMARKS

Claims 46-48, 51-56, and 58-81 are pending in this application. Claims 46, 51, 56, 62, 63, 72, and 75-81 have been amended. Claim 57 has been cancelled without prejudice to the underlying subject matter. Claims 49 and 50 were previously cancelled without prejudice to the underlying subject matter. No new matter has been introduced.

The drawings stand objected to under 37 C.F.R. § 1.83(a) for failing to show every feature of the invention specified in the claims. Specifically, the Examiner asserts that the drawings do not "show every feature of the invention specified in the claims." (Office Action at 2). In particular, the Examiner states that the drawings must show "a conductive path extending from said buried conductor pattern wherein said buried conductor pattern has a spherical pattern;" "at least one buried conductor pattern having a pipe-shaped pattern, further comprising a second buried conductor pattern having a spherical pattern;" "at least two buried conductor patterns, wherein a first of said at least two buried conductor patterns is located below a second of said at least two buried conductor patterns and relative to a surface of said monocrystalline substrate, and a first conductive path extending from said first of said at least two buried conductor patterns, wherein said at least one of buried conductor patterns has a spherical pattern." (Office Action at 2).

Applicants have submitted Figure 14A which depicts three buried conductor patterns 71, 81 and 91 located within substrate 10. A first plate-shaped conductor pattern 91 is at a level above a second spherical conductor pattern 81 and a pipe-shaped conductor pattern 71, relative to a surface 11 of the substrate 10. Applicants have also amended the specification to refer to Figure 14A. For at least the reasons discussed immediately below regarding the compliance of claims 46-48 and 74 with 35 U.S.C. § 112, first paragraph, the specification supports the addition of Figure 14A.

Claims 46-48 and 74 stand rejected under 35 U.S.C. § 112, first paragraph, as "containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claim invention. (Office Action at 3). Specifically, regarding claims 46-48, the examiner states that the "specification does not describe at least one buried conductor pattern having a spherical pattern, and a conductive path extending from said buried conductor pattern." (Office Action at 3). The Examiner also notes that, "[r]egarding claim 74, the specification does not describe at least one buried conductor pattern having a plate-shaped pattern, further comprising a second buried conductor pattern having a pipe-shaped pattern, further comprising a third buried conductor pattern having a spherical pattern." Applicants respectfully traverse this rejection.

Applicants respectfully direct the Examiner's attention to the last paragraph on page 18 of the specification extending to the top of page 19, which, prior to amendment, stated in part that "[a]lthough the buried silicon structure 100 is shown in Figure 14 as comprising only three buried conductor patterns 70, 80 and 90, respectively, it must be readily apparent to those skilled in the art that in fact any number of such buried conductor patterns may be formed on the substrate 10, as pipes, plates, or spheres, by methods of the present invention." (Specification at 18). The text of the specification further emphasizes that "the invention is not limited to a combination of three buried conductor patterns, but any combination of any number of empty-spaced patterns filled with a conductor may be employed, as desired." (Specification at 18-19). More importantly, the specification clearly details on pages 9 through 11 the formation of empty spaces having "various shapes, such as plates, spheres or pipes" (specification at 9-11), as well as the formation of buried conductive patterns from such empty space shapes having conductive paths extending therefrom. (Specification at 15-18).

Accordingly, one of ordinary skill in the art would readily understand that, at the time the present application was filed, Applicants were in possession of the subject matter of claims 46-48 and 74, specifically "at least one buried conductor pattern having a spherical pattern, and a conductive path extending from said buried conductor pattern;" "at least one buried conductor pattern having a plate-shaped pattern, further comprising a second buried conductor pattern having a pipe-shaped pattern, further comprising a third buried conductor pattern having a spherical pattern;" and all other combinations of buried conductor patterns contemplated by the claims. Therefore, Applicants respectfully request the withdrawal of the rejection of claims 46-48 and 74 under 35 U.S.C. § 112.

Claim 51 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite because "[c]laim 51 is dependent on cancelled claim 50." (Office Action at 3). Claim 51 has been amended to depend from amended independent claim 46 and, therefore, is now in compliance with the requirements of 35 U.S.C. § 112, second paragraph.

Claims 46, 52, 54, 56-61, 72 and 75 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Rostoker (U.S. Patent No. 5,662,768) ("Rostoker"). This rejection is respectfully traversed.

The claimed invention relates to semiconductor devices and, in particular, to buried conductors within a monocrystalline substrate. As such, amended independent claim 46 recites an "integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate." Amended independent claim 46 also recites that "at least a portion of a top surface of said buried conductor pattern is below a top surface of said substrate and at least a portion of a bottom surface of said buried conductor pattern is above a bottom surface of said substrate, said at least one buried conductor pattern having a spherical pattern and forming at least a part of an interconnect between devices." Amended independent claim 46 further recites "a conductive path extending from said buried conductor pattern to said devices."

Independent claim 56 recites a buried conductor pattern within a substrate comprising "at least one empty-spaced pattern in said substrate formed by annealing said substrate containing at least one hole drilled therein, said empty-spaced pattern having one of a sphere-shaped, plate-shaped, or pipe-shaped configuration" and "a conductive material filling said empty space pattern such that at least a portion of a top surface of said conductive material is below a top surface of said substrate and at least a portion of a bottom surface of said conductive material is above a bottom surface of said substrate." Amended independent claim 56 further recites "said buried conductor pattern forming at least a part of an interconnect between devices."

Amended independent claims 72 and 75 recite "an integrated circuit substrate" comprising "at least one buried conductor pattern provided within a monocrystalline substrate such that at least a portion of a top surface of said buried conductor pattern is below a top surface of said substrate and at least a portion of a bottom surface of said buried conductor pattern is above a bottom surface of said substrate." Amended independent claim 72 further recites "said at least one buried conductor pattern having a plate-shaped pattern," whereas amended independent claim 75 further recites "said at least one buried conductor pattern having a pipe-shaped pattern."

Rostoker relates to "methods of forming high surface area trenches by etching through a substrate having chemically distinct strata." (Col 1, lines 8-10). According to Rostoker, "trenches may electrically isolate MOS devices from one another on integrated circuits" or "serve as part of a capacitor in 'trench capacitor type' dynamic random access memory chips." (Col. 1, lines 11-16). To form a trench capacitor, Rostoker teaches that impurity species are implanted into the substrate "so as to create one or more layers 10 that alternate with unimplanted substrate material 4." (Col 5; lines 15-21; Fig. 1b). Rostoker also teaches that a "preferential etch preferentially removes the impurity-implanted areas with respect to the unimplanted substrate, to form a lateral indentation 16 in the trench sidewalls where the top layer of

impurity was implanted." (Col. 6, lines 8-11; Fig. 1e; Fig. 1f). Rostoker notes that "some nonlinearity (high surface area) is introduced in the trench sidewalls" (Col. 6, lines 38-40) and that the sidewalls may be rounded. (Col. 9, lines 23-27). Rostoker further teaches that the "capacitor region includes a layer of oxide 31 or other dielectric conformally deposited on an undulating trench sidewall" (col. 8, lines 61-66) and that the "region of substrate 4 lying immediately beyond the dielectric layer 31 forms one plate of the trench capacitor" while a "plug of polysilicon 32 fills the trench and forms a second plate of the trench capacitor." (Col. 8, line 67; Col. 9, lines 1-3; Fig. 3).

Rostoker does not disclose all limitations of claims 46, 52, 54, 56-61, 72 and 75. Rostoker does not teach or suggest a "buried conductor pattern" "forming at least a part of an interconnect between devices," as recited in amended independent claims 46, 56, 72 and 75. As noted above, Rostoker teaches "methods of forming high surface area trenches" to "electrically *isolate* MOS devices from one another on integrated circuits" or "serve as *part of a capacitor.*" (Col. 1, lines 5-16, emphasis added). Thus, Rostoker does not teach or suggest a "buried conductor pattern forming at least a part of an *interconnect between devices*," as recited in amended independent claim 56, much less a buried conductor pattern having a "spherical pattern," "plate-shaped pattern" or "pipe-shaped pattern," as recited in amended independent claim 46, 72 and 75, respectively (emphasis added). For at least these reasons, withdrawal of the rejection of claims 46, 52, 54, 56-61, 72 and 75 is respectfully requested.

Claims 46, 52, 54-61, 72 and 75 are rejected under 35 U.S.C. § 102(b) as being anticipated by Lu et al. (U.S. Patent No. 5,943,581) ("Lu"). This rejection is respectfully traversed.

Lu relates to a method of fabricating a dynamic random access memory (DRAM) cell utilizing a "buried N+ doped region in a silicon substrate which is removed by selective etching to form a cavity," which "is then coated with a dielectric layer and filled with a polysilicon to form a horizontally extending buried reservoir storage capacitor." (Col. 1, lines 17-23).

Lu does not disclose all limitations of claims 46, 52, 54-61, 72 and 75. Lu does not teach or suggest an "integrated circuit substrate comprising at least one buried conductor pattern provided within a monocrystalline substrate," "said at least one buried conductor pattern having a *spherical* pattern," as amended independent claim 46 recites (emphasis added). As noted above, Lu discloses a "*horizontally extending* buried reservoir storage capacitor" (col. 1, lines 22-23) and not a "buried conductor pattern *having a spherical pattern*," as amended independent claim 46 recites (emphasis added). Lu clearly emphasizes that "polysilicon layer 28 is deposited to a thickness sufficient to fill the hole 4," and that the hole 4 has a *width*. (Col. 7, lines 45-56). Therefore, it would be impossible for Lu's polysilicon layer 28 to have a spherical shape.

Lu also does not teach or suggest a "buried conductor pattern" wherein "at least a portion of a top surface of said buried conductor pattern is below a top surface of said substrate and at least a portion of a bottom surface of said buried conductor pattern is above a bottom surface of said substrate," as recited in amended independent claims 46, 72, and 75. Similarly, Lu does not teach or suggest a "buried conductive pattern" comprising *inter alia* "a conductive material filling said empty space pattern such that at least a portion of a top surface of said conductive material is below a top surface of said substrate and at least a portion of a bottom surface of said conductive material is above a bottom surface of said substrate," as recited in amended independent claim 56.

According to Lu, an epitaxial layer is grown over a substrate having an N+ doped region. A hole is etched in the epitaxial layer to the N+ region and the N+ region is removed resulting in a cavity "for the buried reservoir capacitor." (Col. 7, lines 6-21. Accordingly, Lu shows that the epitaxial layer forms a top boundary for the cavity. (FIG. 6). Lu further teaches forming a polysilicon layer on inner surfaces of the cavity. (Col. 7, lines 45-27). Thus, Lu cannot teach that "at least a portion of a top surface of said buried conductor pattern is below a top surface of said substrate," as recited in amended independent claims 46, 72, and 75; nor can Lu teach "a conductive material filling said empty space pattern such that at least a portion of a top surface of

said conductive material is below a top surface of said substrate," as recited in amended independent claim 56.

Moreover, Lu is silent about a "buried conductor pattern" "forming at least a part of an interconnect between devices," as recited in amended independent claims 46, 56, 72 and 75. Lu only teaches depositing a polysilicon layer in a cavity to form a capacitor for a DRAM cell. Accordingly, Lu fails to teach or suggest all the limitations of claims 46, 52, 54-61, 72 and 75, and withdrawal of the rejection of these claims is respectfully requested.

Claims 46-48, 52, 61, and 72-75 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ohtsuki (U.S. Patent No. 5,629,226) ("Ohtsuki") in view of Yamagata et al. (U.S. Patent No. 5,679,475) ("Yamagata"). This rejection is respectfully traversed.

Ohtsuki relates to a "buried plate type DRAM and a method of manufacturing the same." (Col. 1, lines 14-16). According to Ohtsuki, a substrate is etched to form a trench, which may include an upper portion like a cylinder shape and a lower portion like a sphere, diamond, or triangle flask. (Col. 6, lines 50-54; Col. 7, lines 50-53). Ohtsuki teaches forming a first conductive layer on the inner surface of the trench, forming an insulating layer on the first conductive layer, and then filling the trench with a conductive material to form a capacitor. (Col. 4, lines 17-23).

Yamagata relates to a "process for preparing an SOI semiconductor substrate by bonding and a semiconductor substrate obtained by the process." (Col. 1, lines 12-14). Yamagata discloses an SOI substrate structure for use with various high performance electronic devices. (Col. 3, lines 48-59).

The subject matter of claims 46-48, 52, 61, and 72-75 would not have been obvious over Ohtsuki in view of Yamagata, whether considered alone or in combination. Specifically, the Office Action fails to establish a *prima facie* case of obviousness. Courts

have generally recognized that a showing of a *prima facie* case of obviousness necessitates three requirements: (i) some suggestion or motivation, either in the references themselves or in the knowledge of a person of ordinary skill in the art, to modify the reference or combine the reference teachings; (ii) a reasonable expectation of success; and (iii) the prior art references must teach or suggest all claim limitations. See e.g., In re Dembiczak, 175 F.3d 994, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999); In re Rouffet, 149 F.3d 1350, 1355, 47 U.S.P.Q.2d 1453, 1456 (Fed. Cir. 1998); Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc., 75 F.3d 1568, 1573, 37 U.S.P.Q.2d 1626, 1630 (Fed. Cir. 1996). Importantly, the teaching or suggestion to make the claimed combination and the reasonable expectation for success must both be found in the prior art and not based on the Applicants' disclosure. M.P.E.P. § 2142.

In the present case, Ohtsuki and Yamagata, alone or in combination, fail to teach or suggest a "buried conductor pattern" that forms "at least a part of an interconnect between devices," as recited in amended independent claims 46, 56, 72, and 75. Ohtsuki teaches only a capacitor formed in a trench having a top cylinder like portion and a bottom sphere, diamond, or triangle flask like portion. (Col. 6, lines 50-54; Col. 7, lines 50-53). Yamagata is silent about a buried conductor pattern, much less about a "buried conductor pattern" "forming at least a part of an interconnect between devices," as in the claimed invention. Accordingly, Ohtsuki, even when considered in combination with Yamagata, does not teach or suggest all the limitations of amended independent claims 46, 56, 72, and 75. For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness, and withdrawal of the rejection of claims 46-48, 52, 61 and 72-75 is respectfully requested.

Claims 46, 51, 52, 72 and 75 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki et al. (U.S. Patent No. 5,176,789) ("Yamazaki") in view of Yamagata. This rejection is respectfully traversed.

Yamazaki "relates to a capacitor for a semiconductor memory, and to a method in which a photo CVD process is carried out so that the deposition is effectively

performed also on insides of depressions." (Col. 1, lines 13-16). Yamazaki discloses "a semiconductor device in which a cave is formed in a trench to increase the capacitance formed in the trench." (Col. 4, lines 56-57; Figs. 5(A)-(C)). Yamazaki teaches that "an anisotropic etching [is] carried out to perform a lateral etching so that a cave 40 is formed." (Col. 5, lines 1-2). Yamazaki further teaches that a conductive layer is deposited on inside walls of the cave and that "the cave is desirably formed, in order to increase the inner surface area, like the low portion of a wine-glass," or "the lower profile of the cave may be elongated only in one horizontal direction." (Col. 5, lines 5-15, 53-58; Figs. 7(A)-(D)).

The subject matter of claims 46, 51, 52, 72 and 75 would not have been obvious over Yamazaki in view of Yamagata. The cited references, whether considered alone or in combination, fail to teach or suggest all limitations of amended independent claims 46 and 56. Yamazaki is silent about a "buried conductor pattern *having a spherical pattern*," as amended independent claim 46 recites (emphasis added). Moreover, Yamagata is silent about any buried conductor pattern, much less about a "buried conductor pattern having a spherical pattern," as in the claimed invention.

Yamazaki and Yamagata are also silent about a "buried conductor pattern" "forming at least a part of an interconnect between devices," as recited in amended independent claims 46, 56, 72 and 75. Yamazaki teaches only a cave having a conductive layer on inside walls for increased capacitance which may be part of a capacitor for a semiconductor memory, and not a "buried conductor pattern" "forming at least a part of an interconnect between devices," as in the claimed invention. Yamagata is silent about any buried conductor pattern and cannot overcome Yamasaki's deficiencies. Accordingly, Yamazaki, even when considered in combination with Yamagata, does not teach or suggest all the limitations of independent claims 46, 56, 72 and 75, and of dependent claims 51 and 52. For at least these reasons, the subject matter of claims 46, 51, 52, 72, and 75 would not have been obvious over Yamazaki and Yamagata, and withdrawal of the rejection of these claims is respectfully requested.

Claims 72, 73, 75-79 and 81 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Livengood et al. (U.S. Patent No. 6,495,454 B2) ("Livengood") in view of Yamagata. This rejection is respectfully traversed.

Amended independent claim 76 recites "an integrated circuit substrate comprising first and second buried conductor patterns provided within a monocrystalline substrate such that at least a portion of a top surface of each of said buried conductors pattern is below a top surface of said substrate and at least a portion of a bottom surface of each of said buried conductor patterns is above a bottom surface of said substrate." Amended independent claim 76 also recites that the first and second buried conductive patterns form "at least a part of first and second interconnects between devices, respectively" and that the first buried conductor pattern "is located below said second buried conductor pattern and relative to said surface of said monocrystalline substrate." Amended independent claim 76 further recites "a first conductive path extending from said first buried conductor pattern and a second conductive path extending from said second buried conductor pattern."

Livengood relates to "interconnection structures that include the substrate of an integrated circuit." (Col. 1, lines 12-13). Livengood discloses a backside interconnect structure "used to deliver power through the substrate to the front side of an integrated circuit." (Col. 1, lines 44-46). Livengood teaches that "power planes are formed on the back side of a substrate, and a series of deep vias through the substrate are used to couple the power planes to front side metal lines, and to well taps." (Col. 1, lines 47-50).

The subject matter of claims 72, 73, 75-79 and 81 would not have been obvious over Livengood in view of Yamagata. Neither Livengood nor Yamagata, whether considered alone or in combination, teaches or suggests all limitations of amended independent claims 72, 75 or 76. Livengood teaches a series of deep vias *through* the substrate to couple power planes on the back side of the substrate to metal lines on the front side of the substrate and well taps. (Col. 1, lines 47-50). Livengood

teaches that the vias are formed by etching the substrate through openings in a mask layer to form "a substantially *vertical* pathway" from the front side of the substrate to the back side of the substrate. (Col. 8, lines 3-16, 40-43; emphasis added). Thus, Livengood teaches that top surfaces of the vias are connected to metal lines and bottom surfaces of the vias are connected to power planes. Livengood does not teach or suggest "at least one buried conductor pattern provided within a monocrystalline substrate such that at least a portion of a top surface of said buried conductor pattern is below a top surface of said substrate and at least a portion of a bottom surface of said buried conductor pattern is above a bottom surface of said substrate" (claims 72 and 75), much less "first and second buried conductor patterns provided within a monocrystalline substrate such that at least a portion of a top surface of each of said buried conductors pattern is below a top surface of said substrate and at least a portion of a bottom surface of each of said buried conductor patterns is above a bottom surface of said substrate" (claim 76).

Additionally, because Livengood teaches that the vias are formed by etching the substrate through openings in a mask layer to form "a substantially vertical pathway" from the front side of the substrate to the back side of the substrate (col. 8, lines 3-16, 40-43), Livengood cannot teach or suggest "first and second buried conductor patterns provided within a monocrystalline substrate," "wherein said first buried conductor pattern is located below said second buried conductor pattern and relative to said surface of said monocrystalline substrate," as recited in amended independent claim 76. As noted above, Yamagata is silent about any buried conductor pattern and, therefore, cannot overcome Livengood's deficiencies. For at least these reasons, the subject matter of claims 72, 73, 75-79 and 81 would not have been obvious over Livengood in view of Yamagata, and Applicants respectfully request withdrawal of the rejection of these claims.

Claims 62-71 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rostoker as applied to claims 46, 52, 54, 56-61, 72, and 75 in view of Tsu et al.

(U.S. Patent No. 6,294,420 B1) ("Tsu"). This rejection is respectfully traversed.

Independent claim 62 recites "a processor system comprising a processor and a circuit coupled to said processor," at least one of said circuit and processor comprising "a conductive structure comprising a substrate having at least one empty space pattern formed by annealing said substrate having at least one hole drilled therein." Independent claim 62 also recites that the empty-spaced pattern has "one of a sphere-shaped, plate-shaped, or pipe-shaped configuration" and that "a conductive material" fills the empty space pattern "such that at least a portion of a top surface of said conductive material is below a top surface of said substrate and at least a portion of a bottom surface of said conductive material is above a bottom surface of said substrate, said conductive structure forming at least a part of an interconnect between devices."

Tsu relates to "an integrated circuit capacitor and a method of forming a capacitor." (Col. 1, lines 14-15). Tsu discloses that a capacitor may be used in a DRAM array, and that the memory array may be "embedded in a larger integrated circuit device." (Col. 7, lines 54-62; Col. 8, lines 61-67).

Rostoker and Tsu, whether considered alone or in combination, fail to teach or suggest all the limitations of claims 62-71. For at least the reasons set forth above regarding the patentability of claims 46, 52, 54, 56-61, 72 and 75, Rostoker would not have rendered the subject matter of amended independent claim 62 obvious. Rostoker does not teach or suggest "said conductive structure forming at least a part of an interconnect between devices," as amended independent claim 62 recites. Similarly, Tsu discloses "an integrated circuit capacitor with a polysilicon plug" (col. 5, lines 56-65; Fig. 3a) and not a "conductive structure forming at least a part of an interconnect between devices," as amended independent claim 62 recites. Accordingly, the disclosure of Tsu cannot supplement the inadequacies of Rostoker in this regard. For at least these reasons, the Office Action fails to establish a *prima facie* case of obviousness and withdrawal of the rejection of claims 62-71 is respectfully requested.

Claims 46, 47, 52, 75-78 and 80 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Divakaruni et al. (U.S. Patent No. 6,214,686 B1) ("Divakaruni") in view of Ohtsuki and in further view of Yamagata. This rejection is respectfully traversed.

Divakaruni relates to a "method of fabricating a storage node for a deep trench DRAM on a semiconductor substrate." (Col. 2, lines 13-14). Divakaruni teaches etching adjacent trenches having "bottled shaped" or "bulbous" enlargements to form storage nodes.

The subject matter of amended independent claims 46, 75 and 76 would not have been obvious over Divakaruni in view of Ohtsuki and Yamagata. As noted above, none of Ohtsuki and Yamagata, whether considered alone or in combination, teaches or suggests a "buried conductor pattern" "forming at least a part of an interconnect between devices," as recited in amended independent claims 46 and 75. Additionally, Divakaruni's teachings are insufficient to overcome the deficiencies of Ohtsuki and Yamagata. Divakaruni teaches that a capacitor for a DRAM cell may include a trench having bulbous enlargements, which is filled with *a dielectric* and not with an interconnect material, as in the claimed invention. (Col. 4-5, claim 13). Accordingly, Divakaruni, even when considered in combination with Ohtsuki and Yamagata, does not teach or suggest a "buried conductor pattern" "forming at least a part of an interconnect between devices" (claims 46 and 75), much less "first and second buried conductive patterns forming at least a part of first and second interconnects between devices" (claim 76). For at least these reasons, the subject matter of claims 46, 47, 52, 75-78 and 80 would not have been obvious over these cited prior art references. Applicants respectfully request withdrawal of the rejection of these claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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